ULTRA-DENSE, ULTRA-FAST COMPUTING COMPONENTS: MULTIPLE-VALUE LOGIC CIRCUITS WITH RESONANT TUNNELING BIPOLAR TRANSISTORS

FINAL PROGRESS REPORT

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13. ABSTRACT (Maximum 200 words)

The objective of the program was to develop multiple value logic for a 2:1 reduction in circuit complexity and a 2:1 increase in circuit speed. The approach was to achieve modulo-4 arithmetic in circuits based on resonant tunneling bipolar transistors. Because the multiple value functionality is integrated into the individual devices within the circuits, reductions in circuit complexity and propagation delays may be realized that might not otherwise be achieved. MBE and GSMBE were used to grown epitaxial structures that included AlGaAs-GaAs and InGaP-GaAs heterojunction bipolar transistors integrated with multiple barrier AlAs-GaAs-InGaAs resonant tunnel diodes. Collaborations were with Scientific Research Associates and the University of Michigan for device and circuit design, and with Georgia Tech for device characterization.

Three RTD designs were demonstrated with peak to valley rations of 6 at 300K. An RTBT was fabricated that exhibited a bandwidth of 30 GHz. In addition, a novel epitaxial structure was proposed for a "collector-up" RTBT configuration that will greatly simplify the processing involved in monolithic integration of RTD's and HBT's in multi-valued circuits. Finally, two multi-valued circuits were designed, simulated and tested in hybrid form. These were a 4-step counter and a 4:1 multiple valued multiplexer. Both functioned as designed. The counter, executed with only three transistors and one RTD, would have required more than thirty transistors to implement with binary CMOS logic circuitry.

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Acknowledgments

The authors would like to express their gratitude to members of the faculty and staff of the University of Michigan for numerous contributions, advice and assistance during the course of this work. We thank George Haddad for useful discussions and advice, W.-L. Chen for device processing and characterization and suggestions on device design, and Pinaki Mazumder for proof-of-concept designs and demonstrations of hybrid circuits using quantum devices and multi-valued logic.

List of Figures

Statement of the Problem 1

1.1 BINARY VS. QUATERNARY LOGIC

In the past decade, much research has been done with quantum structures, to explain potential benefits to high speed computing. But is there a near-term application for these structures? Most RTD structures are not faster than the state-of-the-art FET's, but because of the region of negative differential resistance they offer the possibility of increased functionality, combined with simpler device design. In this context we offer the quantum devices as multiple valued logic and memory elements. A recent discussion by Current[1] provides insight into the technological advances required to demonstrate the viability of multiple valued logic. Figure 1-1 displays a 31-input binary adder using binary full adders, and Figure 1-2 displays the same adder but with the binary full adders replaced by quaternary full adders. A parallel counter is a multiple input circuit that counts the number of its inputs that are in a given state, usually ONE. Parallel counters are useful in implementing parallel multipliers, multiple input adders, and digital output correlators.

As shown in Figure 1-1 the inputs are grouped into "threes," and each set of three lines is successively reduced by binary full adders (BFA). Twenty-six BFA's are required for this task, and Current[1] estimates that if each BFA were implemented with ECL using high speed, low power LSI circuits, then thirty-six transistors and resistors would be required.

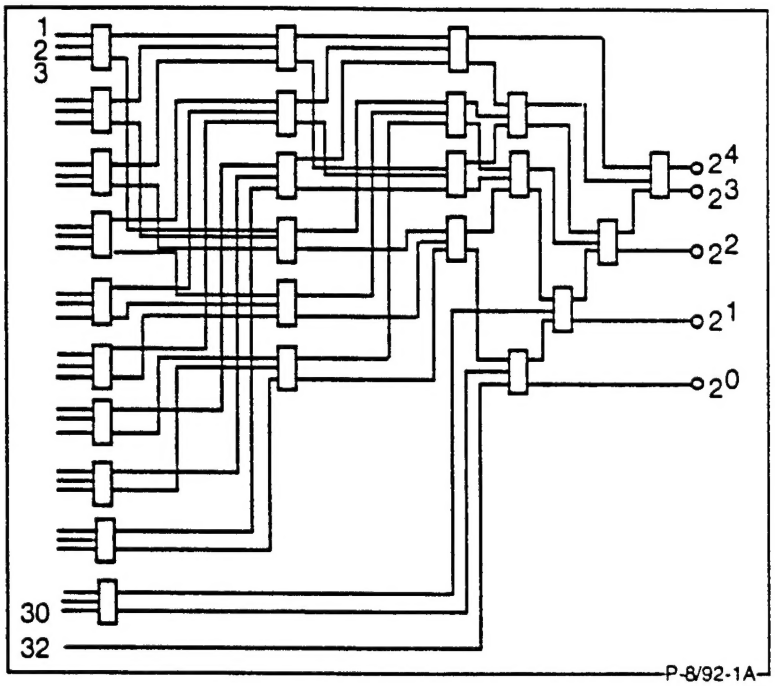


Figure 1-1. Schematic diagram of a 31-input binary parallel counter.

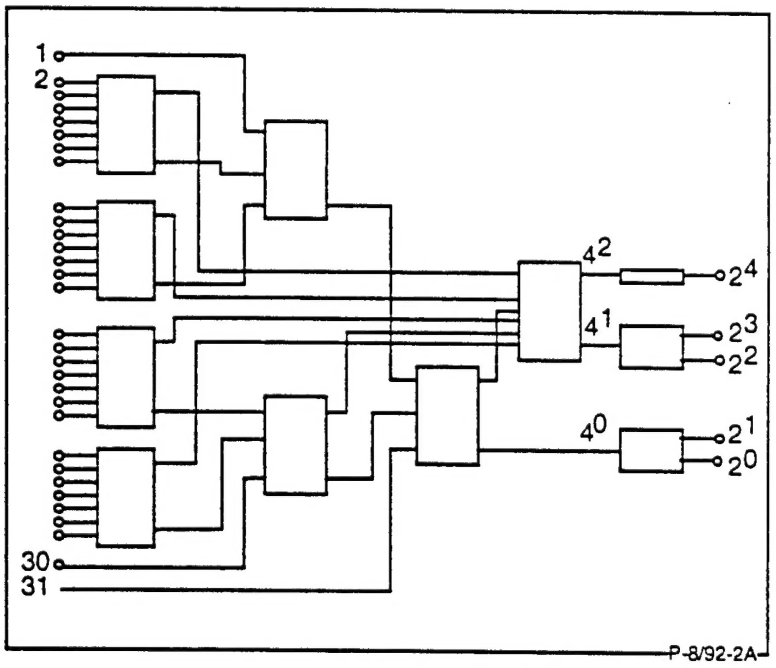


Figure 1-2. Schematic diagram of a 31-input binary parallel counter implemented with QFA's.

The same combinatorial binary counter, implemented with quaternary full adders (QFA), is illustrated in Figure 1-2. Note that the modulo-four outputs are converted to binary ECL compatible voltage outputs. Thus in this picture the QFA is envisioned as replacing an existing BFA. Clearly, systems based entirely upon quaternary logic could be developed. Current[1] envisions forty transistors per QFA but only eight QFA. Thus approximately one-third the number of metal signal lines are required to feed the QFA counter, compared to the BFA counter.

The comparison of the binary implementation to the quaternary implementation should take into account at least three metrics: area, power, and speed. The device count for the quaternary implementation is approximately 35% of the number of devices needed for the binary implementation for combinational circuits and approximately 60% for sequential circuits. This results in a reduced amount of area due to a decreased number of devices and also produces a corresponding reduction in power dissipation. To compare the speed of the binary versus quaternary implementations first examine the number of stages of delay in the combinational implementations in Figures 1-1 and 1-2. The number of stages in the binary implementation is seven, while the quaternary implementation requires five, including the conversion from quaternary to binary at the output. Assuming that the delays for the FA and QFA can be made comparable, the quaternary implementation will have reduced delay over the binary implementation.

In 1990 Current[2] presented a circuit that realizes the QFA with transparent latching with standard polysilicon-gate CMOS technology. Figures 1-3 and 1-4 are sketches of the transfer function of the ideal QFA and the schematic of the CMOS QFA

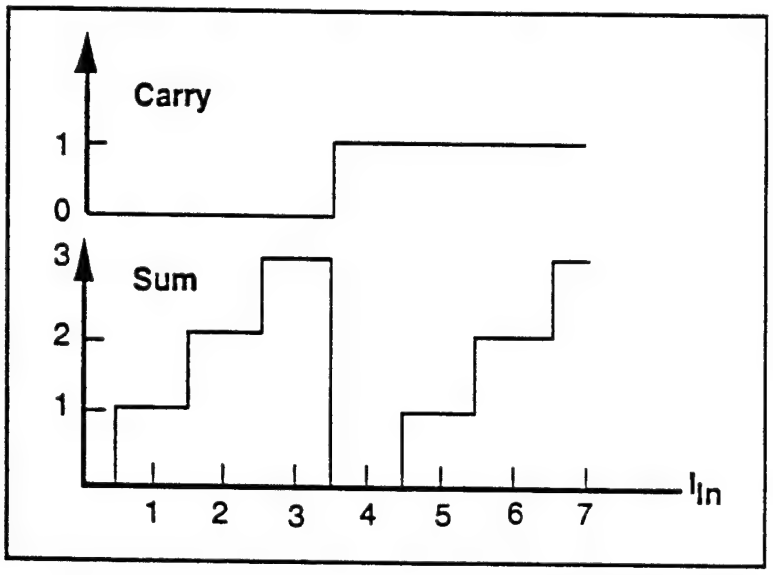


Figure 1-3. DC input-output transfer function of an ideal QFA.

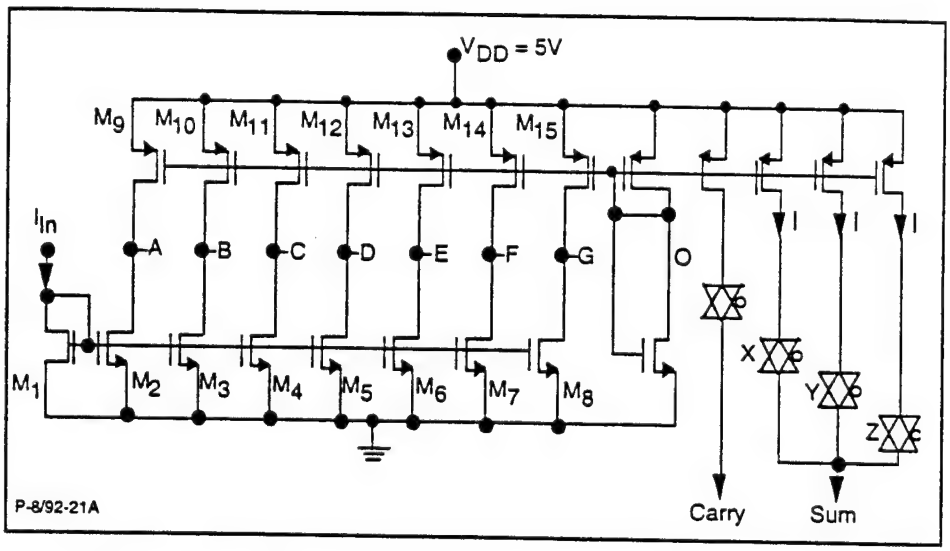


Figure 1-4. QFA circuit schematic using CMOS technology.

circuit. In this discussion Current[2] points out that despite all of the advantages of MVL (fewer operations, gates, transistors, signal lines, etc.), MVL is not used primarily because MVL circuits cannot provide these advantages without corresponding disadvantages, including reduced noise margins and a slower raw switching speed due to increased circuit complexity and functionality. In addition, it has to be proven that MVL improves overall system design. However the Intel 8087 math coprocessor uses a quaternary ROM[3] that provides approximately 31% ROM area savings compared to a binary ROM. No system penalty is incurred because the slower MVL ROM is fast enough to respond within the time budgeted for ROM data lookup. In terms of speed Etiemble, et al[4] discuss the four valued nMOS inverter (shown in figure 1-5) and point out that the inverter was about 13 times slower than the binary inverters. It's important to point out that this deficiency of speed cited in these two examples is not an inherent property of multiple value logic, but related to its implementation using digital devices.

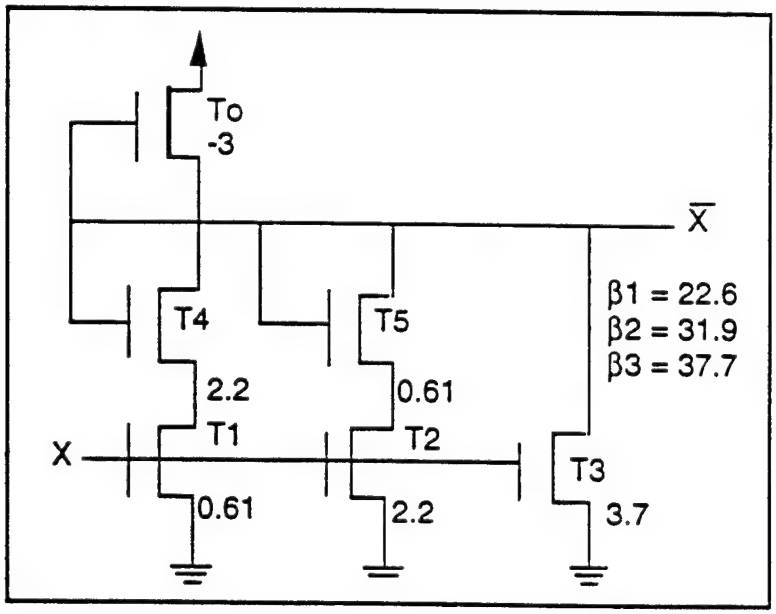


Figure 1-5. Example of an nMOS four-valued inverter.

Let us now return to the statement made earlier that one of the important features of the quantum structures was the presence of negative resistance in the characteristics. Negative resistance devices are not however unique to quantum structures. Indeed Abraham[5] addressed the realization of NDR using FET configuration of Figure 1-6, and of multiple NDR using cascaded FET's as in Figure 1-7.

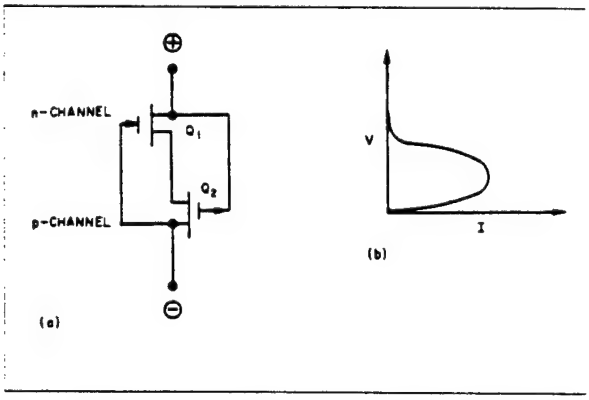


Figure 1-6. FET configuration (a) used to realize single NDR (b).

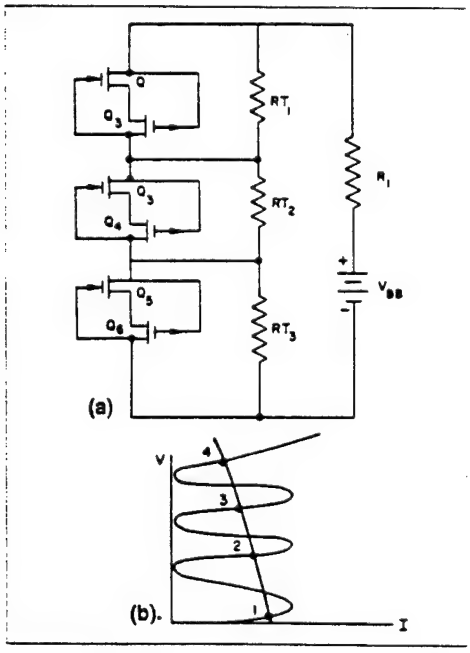


Figure 1-7. Cascaded FET configuration (a) used to realize multiple NDR (b).

1.2 BINARY AND MULTIPLE VALUED LOGIC SIMPLIFICATION USING QUANTUM DEVICES

The first point we notice in dealing with the NDR arising from the quantum devices is that the circuit realization of the NDR is simpler with the quantum devices than with the FET. The resonant tunneling device with NDR is a single two terminal device: NDR with FET's requires two transistors. Six transistors are required for implementation of three NDR regions, plus associated circuitry. In contrast, only one RTBT (with three embedded RTD's) is required to realize three NDR regions. Thus less real estate is required using NDR with RTBT's.

The origin of NDR in RTD's and RTBT's is shown in Figure 1-8. The structure consists of a graded n-type AlGaAs emitter, as indicated, followed by a heavily doped p region in which p-type AlGaAs surrounds a pair of AlAs barriers, which in turn bound an undoped region of GaAs. The collector is a n-type GaAs. In operation electrons with sufficient thermal energy enter the base. Current through the tunnel diode consists of a combination of resonant and non-resonant tunneling. When the base potential is pulled down sufficiently far the resonant current contribution becomes negligible and the base collector current characteristics shown in Figure 1-9 emerge. To achieve multiple regions of negative differential resistance, multiple pairs of resonant tunneling barriers may be embedded in the layer structure, generally in the base or emitter.

The unique feature of the quantum configured devices, either in a two terminal configuration of a three terminal configuration, is thus simplicity in design with fewer transistors. Specifically, higher order logic is easier to configure with quantum structures, and fewer devices are needed to establish the logic operations of higher order

logic. As a consequence the speed characteristics of the logic devices are more likely to approach those of individual devices.

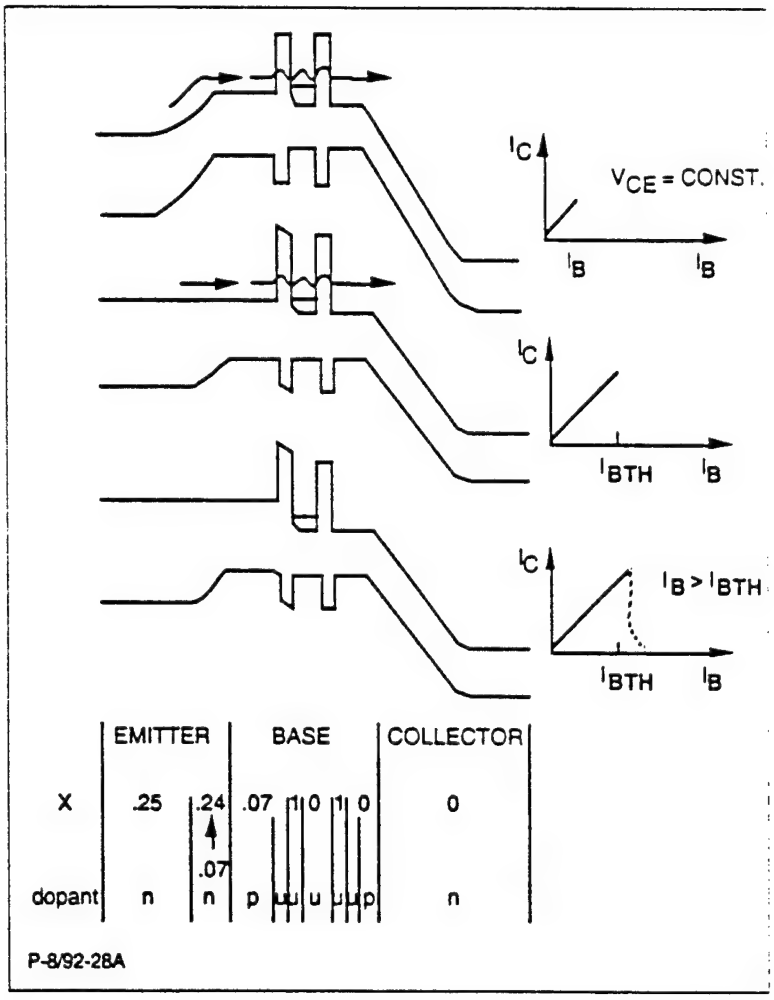


Figure 1-8. Conduction and valence band structure of an HBT with a RTD in the base. Percentage of aluminum is indicated in the legend.

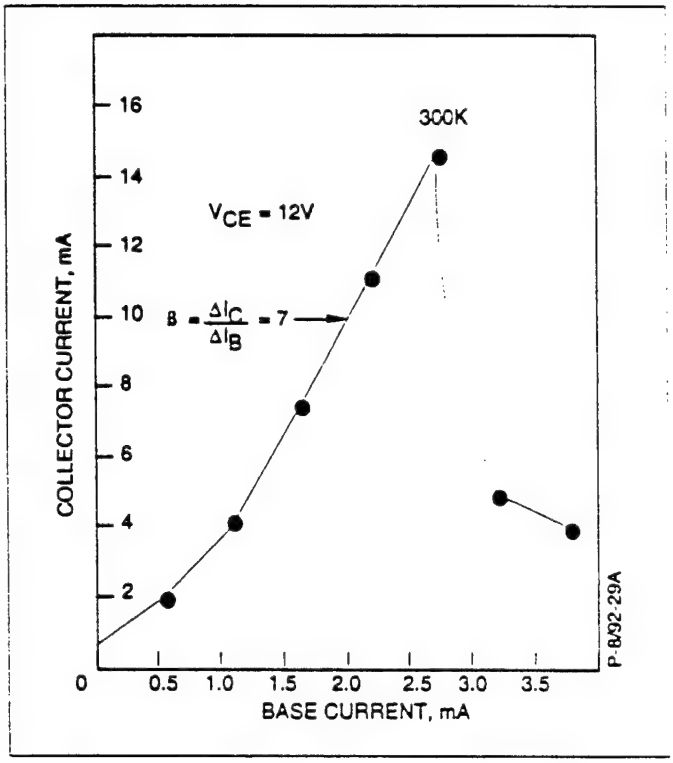


Figure 1-9. Measured collector current versus base current for the RTBT (after Capasso, et al.).

Summary of Results 2

2.1 DEVICE MODELING

A modeling effort was undertaken by H. L. Grubin at SRA to provide designs and physical insights into the operation of the RTBT. To meet this goal, two algorithms were applied to the problem, DEN-MAT and QHD-CAD. Both algorithms were developed prior to the current study, although DEN-MAT was modified for the present program. There were difficulties in dealing with high bias levels and transients in using DEN-MAT and so emphasis at the end of the study involved incorporating QHD-CAD into the study.

We first summarize DEN-MAT (for a review of DEN-MAT see "Density Matrix Simulations of Semiconductor Devices", H. L. Grubin, in *Quantum Transport in Semiconductors,* Edited by D. K. Ferry *et al.,* Plenum Press, New York, 1995.). There were two algorithms used in the study of the RTBT. The first was the density matrix in the coordinate representation. The relevant equation here for electrons:

$$(1)\qquad i\hbar\frac{\partial \rho(\mathbf{x},\mathbf{x}',t)}{\partial t} = -\frac{\hbar^2}{2m}\left(\frac{\partial^2}{\partial \mathbf{x}^2}-\frac{\partial^2}{\partial \mathbf{x}'^2}\right)\rho(\mathbf{x},\mathbf{x}',t)+\left[\left(V(\mathbf{x})-V(\mathbf{x}')\right)-\left(E_F(\mathbf{x})-E_F(\mathbf{x}')\right)\right]\rho(\mathbf{x},\mathbf{x}',t)$$

Here $\rho(\mathbf{x},\mathbf{x}',t)$ is the density matrix in the coordinate representation. The diagonal components (**x=x'**) yield the density. The potential energy is given by $V(\mathbf{x})$, and dissipation id introduced, for a velocity flux density **j**, through the quasi Fermi energy:

$$(2)\qquad E_F(\mathbf{x})-E_F(\mathbf{x}') = -\int_{\mathbf{x}'}^{\mathbf{x}} d\mathbf{x}''\cdot\mathbf{j}/\rho(\mathbf{x}'')m\Gamma(\mathbf{x}'').$$

Equation (1) with a similar one for holes, was solved self-consistently with Poisson's equation.

Figure 1 is a display for a DEN-MAT calculation of the equilibrium band structure used in one of the simulations. A DEN-MAT calculation in which the base potential is unchanged but the collector potential is altered is shown in Figure 2. In addition to the conduction band profile we also display the quasi-Fermi energy. Figure 3 is a DEN-MAT calculation in which the base potential is changed, as indicated, but the collector potential is unaltered from its figure 2 value. Again we are also showing the quasi-Fermi energy. Figures 4 and 5 are similar to figure 3, with the exception of a larger collector voltage. Notice that the current continues to increase.

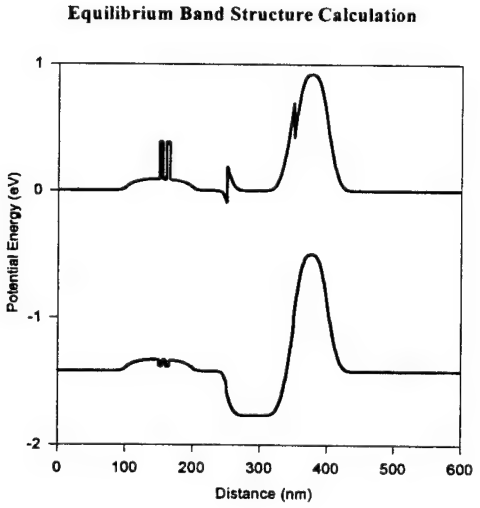


Figure 2-1. DEN-MAT equilibrium band structure calculation.

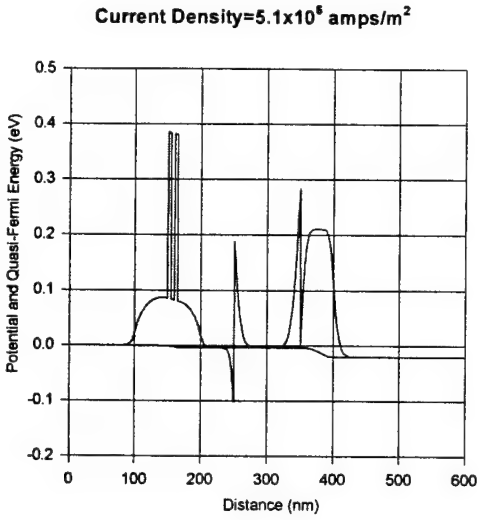


Figure 2-2. DEN-MAT calculation using the same base potential as in Figure 2-1 but a different collector potential. The quasi-Fermi energy is also shown.

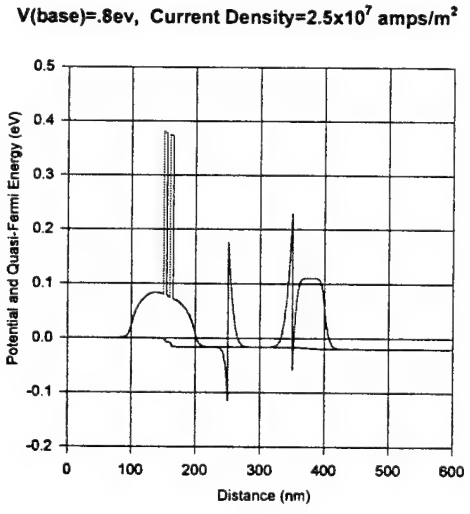


Figure 2-3. DEN-MAT results using the same collector potential as in Figure 2-2 but a different base potential.

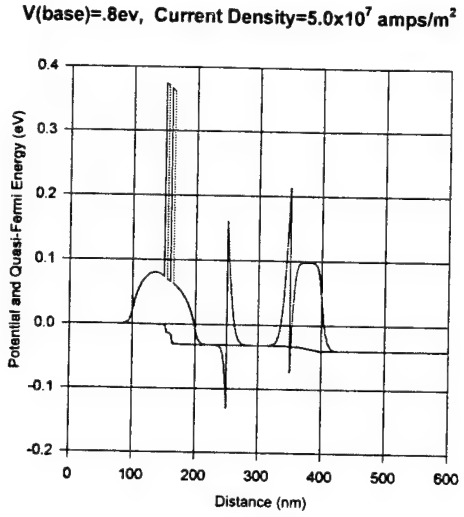


Figure 2-4. Progressing from Figure 2-3, this figure shows the effect of increasing the collector voltage on the DEN-MAT calculation.

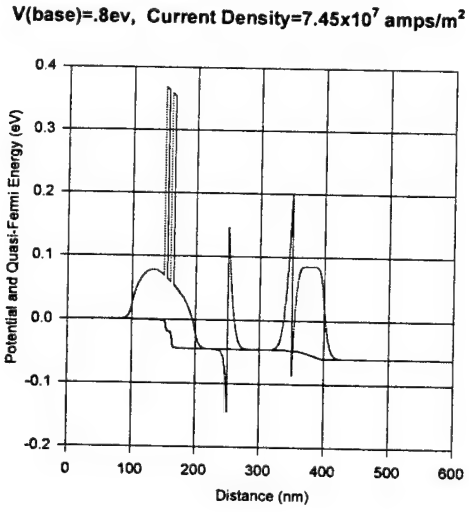


Figure 2-5. The increase in device current with increasing collector voltage is seen in this DEN-MAT calculation at the highest collector potential of the set.

The QHD-CAD or quantum hydro-dynamics algorithm was more successful. Although only single particle transit the software is transient accurate and for the RTBT provided negative conductance. The relevant equations include the continuity equation, Poisson's equation and the momentum and energy balance equations. The latter two are respectively:

$$\frac{\partial\, \rho(x) m v(x)}{\partial t} + \frac{\partial\, \rho(x) m v(x)^2}{\partial x} = -\rho(x)\frac{\partial\left[V(x)+Q(x)/3\right]}{\partial x} - \frac{\partial\, \rho(x) k_B T}{\partial x} - \frac{\rho(x) m v(x)}{\tau} \tag{3}$$

$$\frac{\partial\, E}{\partial\, t} + \frac{\partial\left[v(E+\rho\, k_B T\right]}{\partial\, x} = -\rho(x) v(x)\frac{\partial\left[V(x)+Q(x)/3\right]}{\partial\, x} - \frac{2}{3}\rho(x) Q_W \frac{\partial\, v}{\partial\, x} - \frac{2\left[E-E_0\right]}{\tau} \tag{4}$$

The quantum transport is contained in the Bohm potential:

$$Q \equiv -\left(\frac{\hbar^2}{2m}\right)\frac{\nabla^2\sqrt{\rho(x)}}{\sqrt{\rho(x)}} \tag{5}$$

and the Wigner potential:

$$Q_W(x) = -\frac{\hbar^2}{8m}\,\frac{\partial^2 \ln[\rho(x)]}{\partial x^2} \tag{6}$$

We have implemented the QHD-CAD to examine the RTBT. Figure 6 shows an I-V curve with a region of negative differential conductance for the structure shown in figures 7 and 8. Figure 7 displays the equilibrium charge and potential distribution for a nominal density ($N_{ref} = 10^{18}/cm^3$). Figure 8 shows the distribution under a collector bias

of –400meV. The important point to note is that while this code was not used in the GE program for the design of RTBT, it is capable of providing design information. Further more we have also implemented this code for the RTBT for studying transient accurate switching times, and expect that this part of the code can provide importance circuit information.

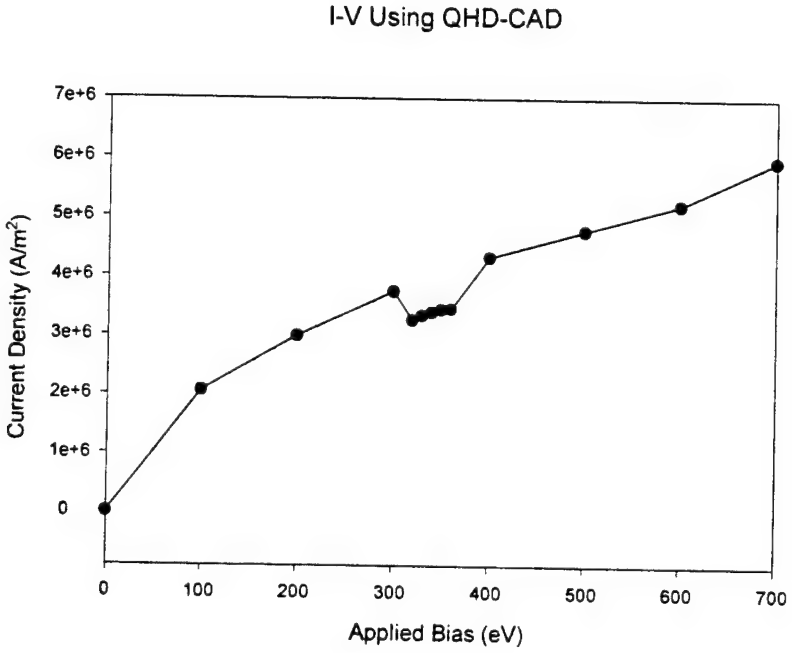


Figure 2-6. QHD-CAD calculation showing negative differential conductance in a RTBT structure.

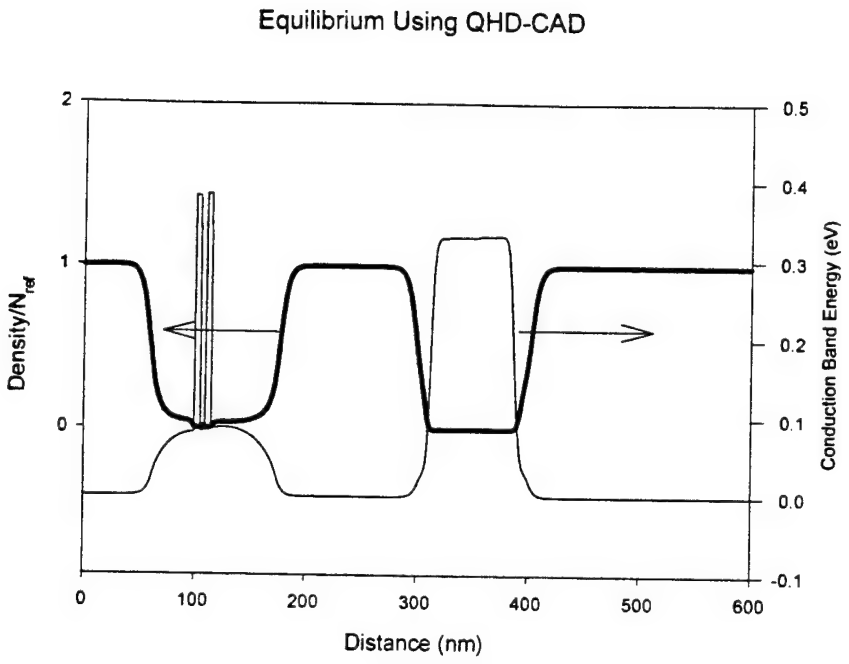


Figure 2-7. Equilibrium charge and potential distribution calculated with QHD-CAD for the structure in Figure 2-6.

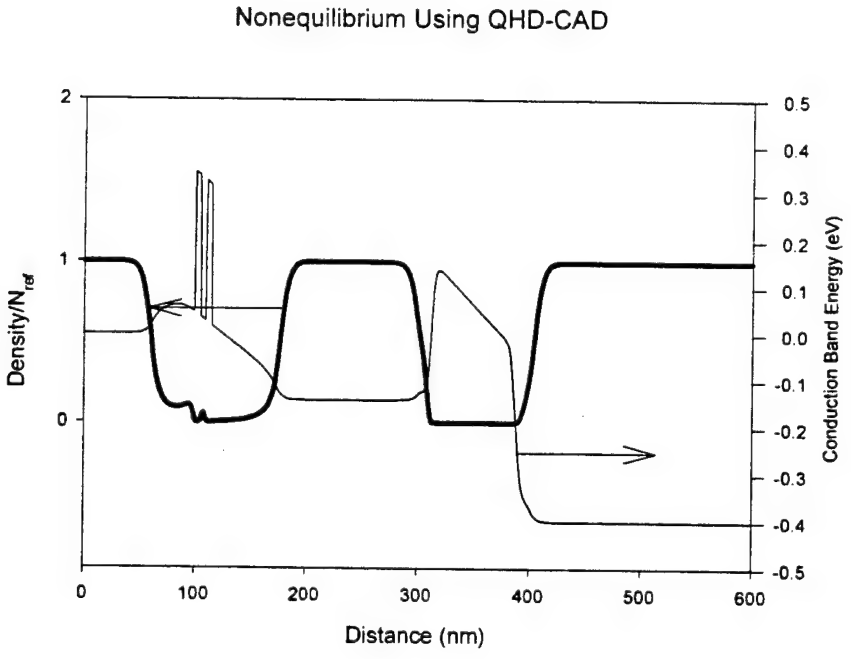


Figure 2-8. QHD-CAD simulation of the charge and potential distribution under a collector bias of -400 meV for the structure in Figure 2-6.

2.2 RTD DEVICE DEVELOPMENT

RTD design, fabrication and characterization were carried out as first steps to realizing MVL circuits. Three RTD structures were considered. The standard RTD structure consists of a GaAs well between two AlAs barriers. The growth sequence for this structure is given in Figure 2-9 along with a simple band diagram. The second RTD structure uses InGaAs to provide a deeper well than in the standard RTD. The deep well design was predicted to reduce the peak voltage of the device by lowering the ground state in the well with respect to the GaAs conduction band. The growth sequence and band structure for this design are shown in Figure 2-10. Finally, the pre-well RTD design depicted in Figure 2-11 was investigated with the intention of reducing the electron energy in the accumulation layer to reduce the valley current, thus increasing the peak-to-valley ratio (PVR) of the device.

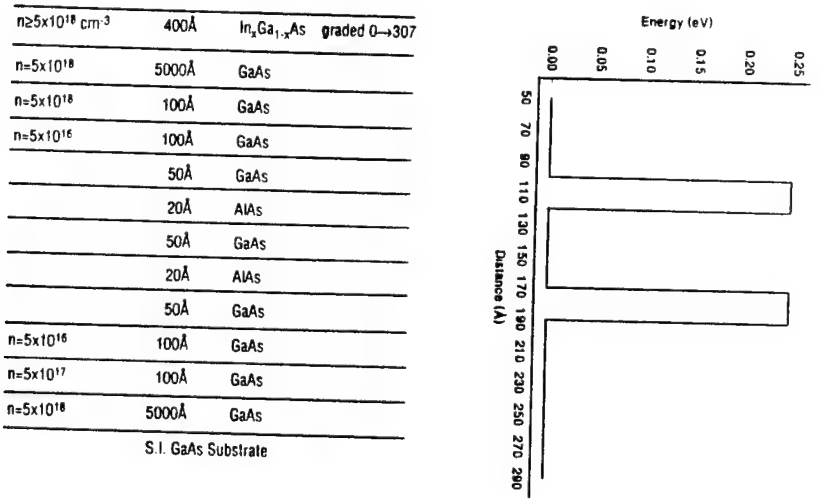


Figure 2-9. MBE growth sequence and conduction band diagram for the "standard" RTD design.

n=5E18	x=0→0.3	400Å	$In_xGa_{1-x}As$
n=4E18		2500Å	GaAs
n=1E18		500Å	GaAs
		30Å	GaAs
		24Å	AlAs
		45Å	$In_{.15}Ga_{.85}As$
		24Å	AlAs
		30Å	GaAs
n=1E18		500Å	GaAs
n=5E18		5500Å	GaAs

S.I. GaAs Substrate

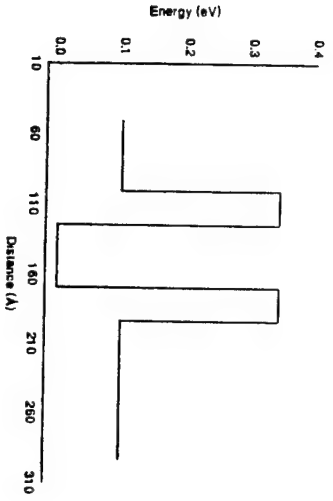


Figure 2-10. MBE growth sequence and conduction band diagram for the "deep well" RTD design.

n=5E18	x=0→0.3	400Å	$In_xGa_{1-x}As$
n=4E18		5000Å	GaAs
n=2E17		100Å	GaAs
		50Å	GaAs
		50Å	$In_{.15}Ga_{.85}As$
		5Å	GaAs
		17Å	AlAs
		5Å	GaAs
		40Å	$In_{.15}Ga_{.85}As$
		5Å	GaAs
		17Å	AlAs
		5Å	GaAs
		50Å	$In_{.15}Ga_{.85}As$
		50Å	GaAs
n=2E17		100Å	GaAs
n=4E18		5500Å	GaAs

S.I. GaAs Substrate

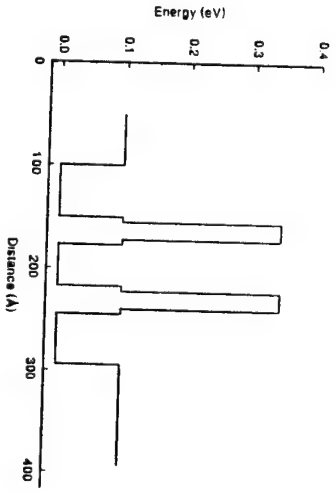


Figure 2-11. MBE growth sequence and conduction band diagram for the "pre-well" RTD design.

All three RTD structures were grown by MBE at Lockheed Martin. Processing and characterization of the devices was carried out at Lockheed Martin and the University of Michigan. Room temperature I-V measurements for the standard RTD are shown in Figure 2-12. The 3 x 5 μm device exhibits a PVR of 6.22 with a peak voltage of 0.96 V. PVR(+) was found to decrease with increasing device area, with ~ 5 being the lowest PVR(+) observed for devices from this wafer. Figure 2-13 presents the 300K I-V characteristics of a deep well RTD. As expected, the peak voltage of 0.27 V is lower than that observed for the standard structure. However, the PVR(+) has dropped to ~ 3.03. The I-V characteristics of the pre-well structure fall between those of the standard and deep well devices with a PVR(+) of ~ 4.37 and a peak voltage of 0.62 V, as seen in Figure 2-14.

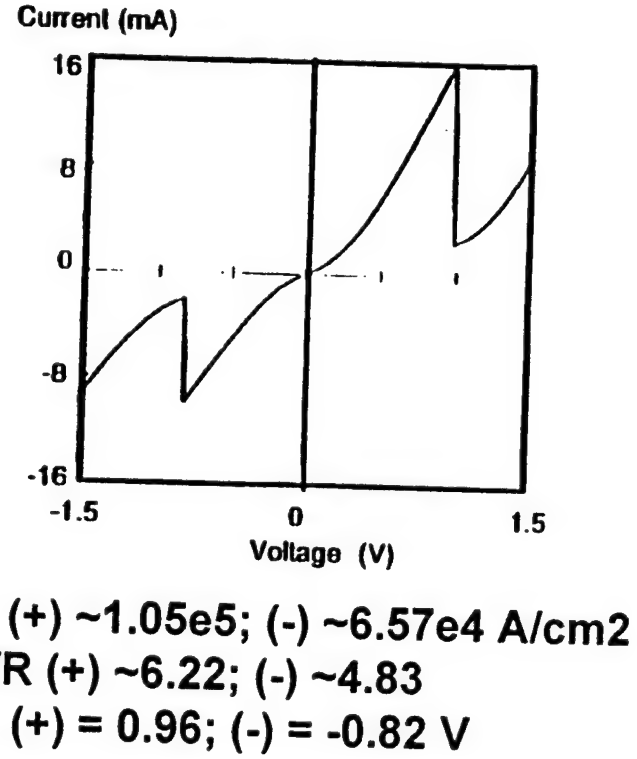


Figure 2-12. I-V characteristics of a "standard" RTD showing a maximum peak-to-valley ratio of > 6.

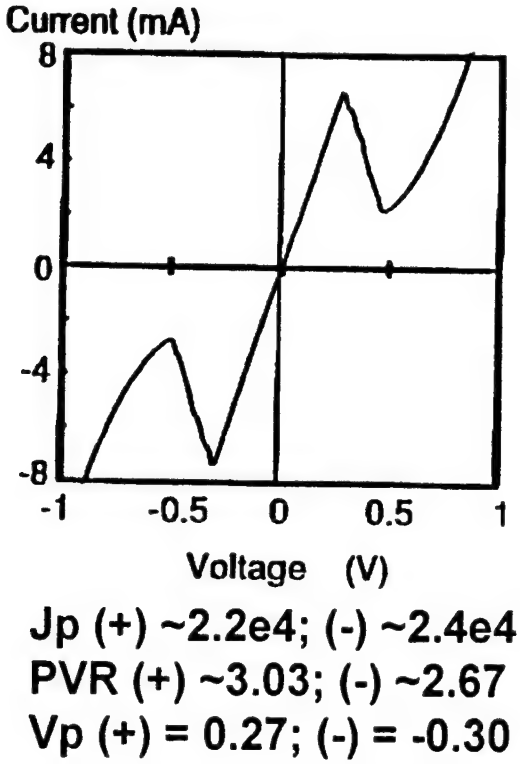


Figure 2-13. I-V characteristics of a "deep well" RTD exhibiting lower peak voltage but decreased PVR.

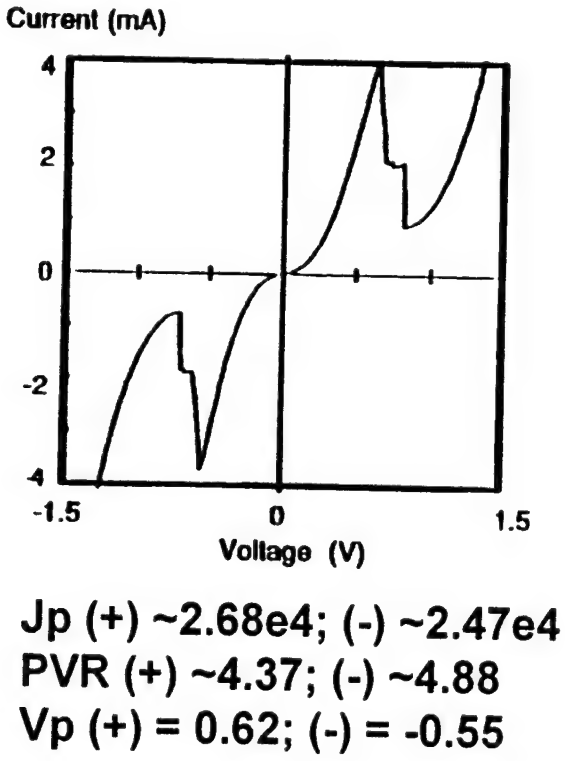


Figure 2-14. I-V characteristics of a "pre-well" RTD with lower peak voltage than the "standard" structure and a PVR of ~ 4.37.

The double-barrier RTD's described above produce 2-peak I-V characteristics. Additional peaks, corresponding to separate logic levels, can be achieved by epitaxially stacking two or more RTD's. Figure 2-15 shows the room temperature I-V characteristics of a stack of two double-barrier AlAs-GaAs-AlAs RTD's exhibiting three state behavior. The 300K I-V curve for a four state device is shown in Figure 2-16. This device consists of a stack of three RTD's.

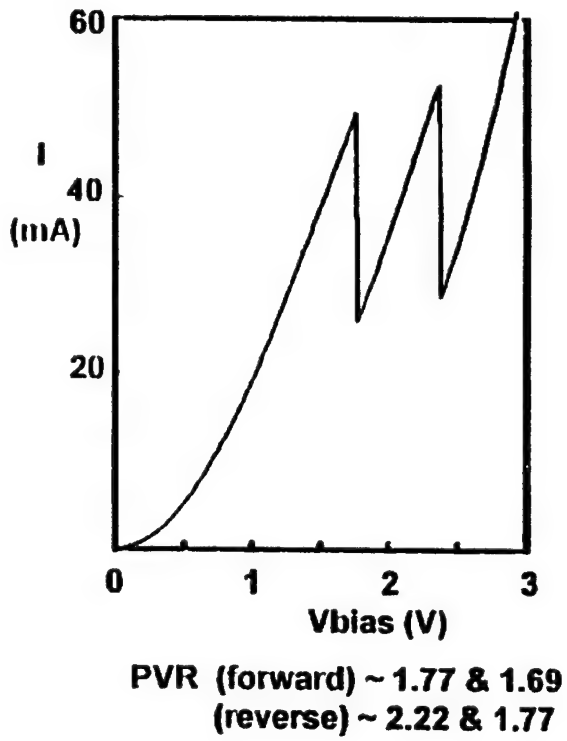


Figure 2-15. I-V curve for a double RTD showing three-state behavior.

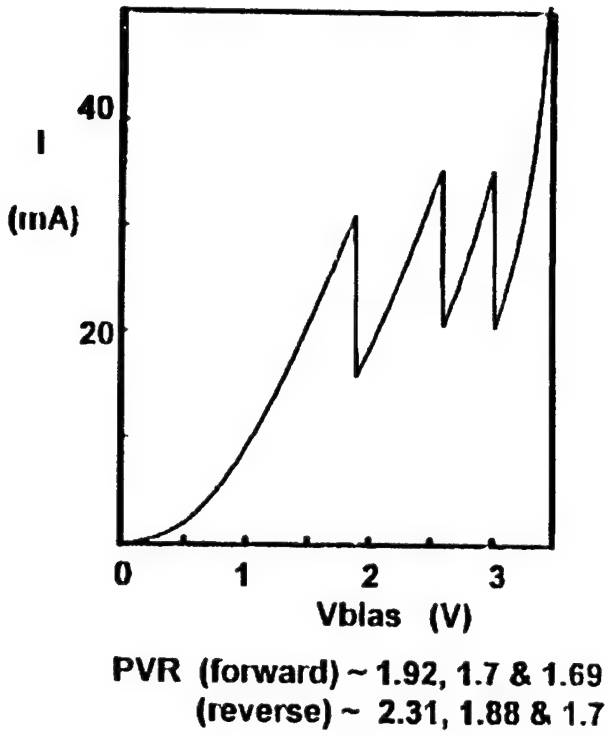


Figure 2-16. I-V curve for a triple RTD structure exhibiting four-state behavior.

2.3 RTBT DEVICE DEVELOPMENT

As discussed in the statement of the problem section, implementing a four-state, NDR circuit with FET's requires six transistors. The same function can be achieved with a single HBT with three embedded RTD's. Thus, the use of RTBT's reduces circuit device count and power dissipation while saving real estate. Figure 2-17 shows the MBE growth sequence and energy band diagram for an RTBT incorporating a single RTD in the emitter of the HBT. Devices were grown and processed at Lockheed Martin and characterized at Georgia Tech. Figure 2-18 is a scanning electron micrograph showing the layout of a fabricated 1 x 10 μm RTBT. This particular structure uses dual emitter fingers (1 x 10 μm), a 1 μm base width and 0.5 μm spacing.

n=1E19	x=0→0.3	400Å	$In_xGa_{1-x}As$	Graded Contact
n=5E18		1000Å	GaAs	Contact
n=1E18		600Å	GaAs	
Undoped		50Å	GaAs	Spacer
Undoped		20Å	AlAs	Barrier
Undoped		45Å	$In_{.15}Ga_{.85}As$	Well
Undoped		20Å	AlAs	Barrier
Undoped		50Å	GaAs	Spacer
n=1E18		600Å	GaAs	
n=5E17	x=0.24-0	100Å	$Al_xGa_{1-x}As$	Graded
n=5E17		300Å	$Al_{0.24}Ga_{0.76}As$	Emitter
Undoped		50Å	GaAs	Spacer
p=4E19		800Å	GaAs	Base
n=5E16		4000Å	GaAs	Collector
n=5E18		6000Å	GaAs	Sub-Collector
S.I. GaAs Substrate				

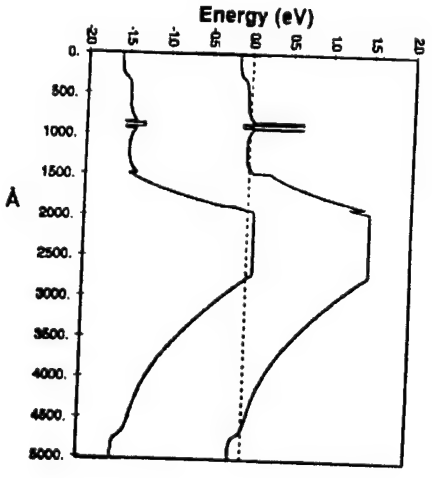


Figure 2-17. MBE layer structure and band diagram of an RTBT consisting of an AlGaAs-GaAs HBT with a single RTD on the emitter side.

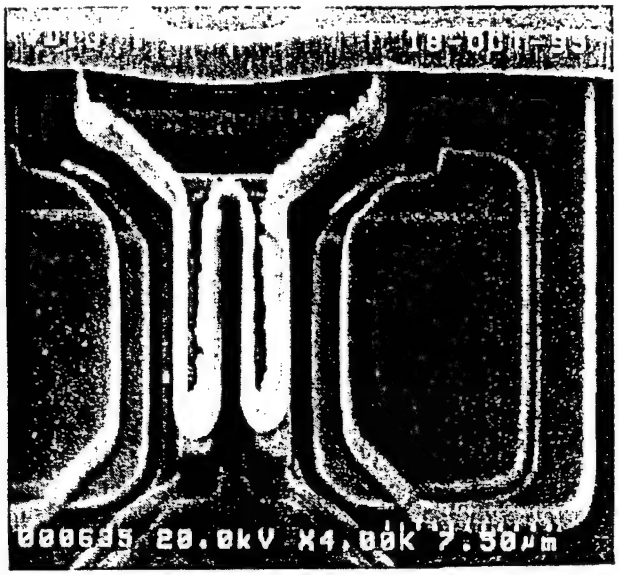


Figure 2-18. SEM micrograph of a processed RTBT based upon the structure in Figure 2-9.

NDR behavior is clearly observed in Figure 2-19 which shows the I-V characteristics of an RTBT with 10 x 10 µm emitter area. The device exhibited a maximum current gain of ~ 48.8 and a peak to valley ratio of ~ 3.1. RF data are presented in Figure 2-20 in which an f_t of ~ 31 GHz and an f_{max} of ~ 42 GHz are observed for this GaAs-based RTBT. f_{max} was also measured as a function of temperature and bias. This data is shown in Figure 2-21. The detailed characterization data collected were used to generate RTBT device models employed in circuit design.

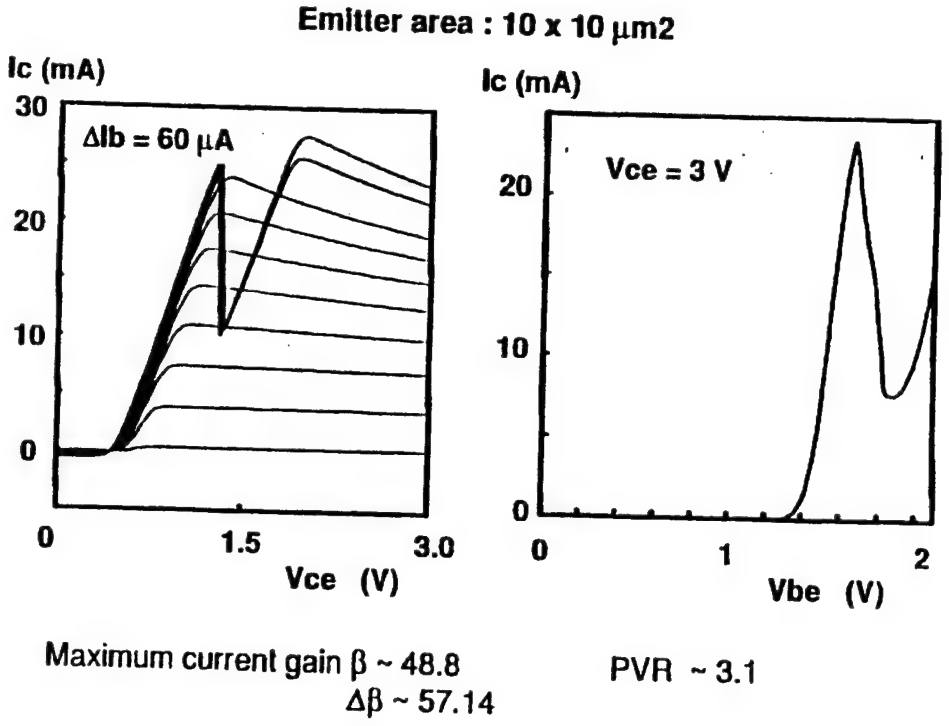


Figure 2-19. I-V characteristics of RTBT showing NDR behavior and a PVR of ~ 3.1.

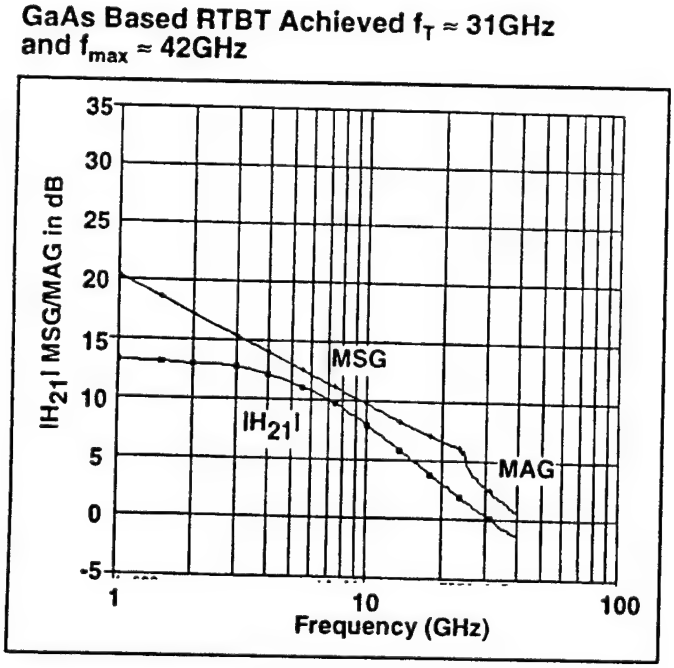


Figure 2-20. RF data for an RTBT demonstrating f_t ~ 31 GHz and f_{max} ~ 42 GHz.

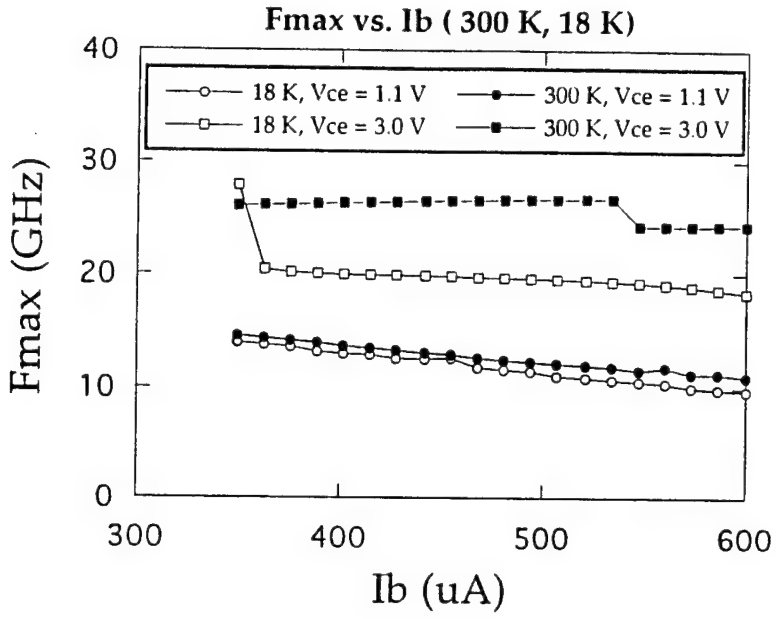


Figure 2-21. Temperature and bias dependence of f_{max} for the processed RTBT.

A novel "collector-up" RTBT design was developed to address problems of integration and device isolation associated with conventional RTBT designs. The growth sequence for the new structure is given in Figure 2-22 and shows the reverse order of epitaxial layers compared to the device detailed in Figure 2-17. By placing the HBT structure on top, selective etches for the removal of AlGaAs can be used to achieve high uniformity in the RTD's. A cross-section of the proposed "collector-up" structure after processing is provided in Figure 2-23. The figure shows the use of flipside vias and the straight-forward deep implant for isolation of the RTD's and HBT. This design should provide significant improvements in the level of integration achievable for multi-valued logic circuits.

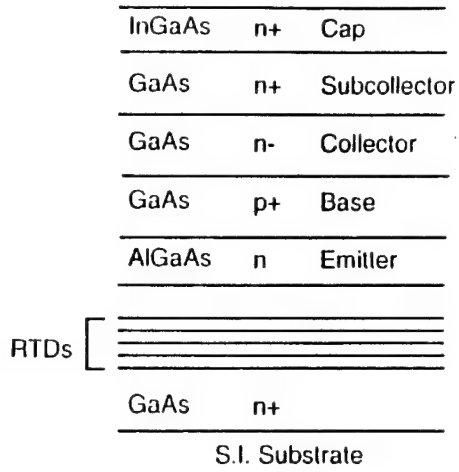


Figure 2-22. Layer structure of the proposed "collector-up" RTBT.

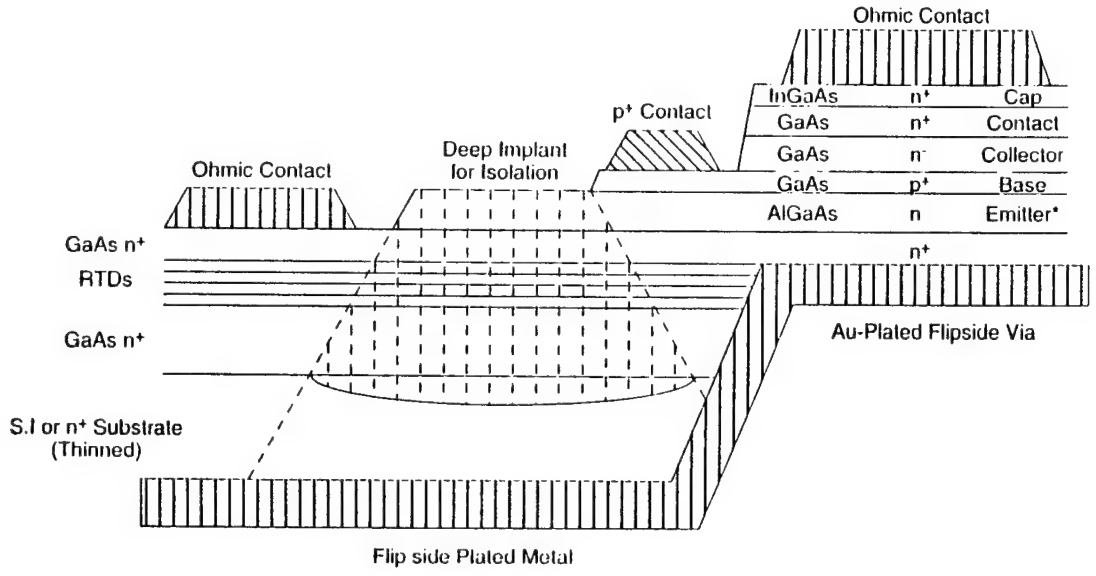


Figure 2-23. Post-processing cross-section of the proposed "collector-up" RTBT showing the use of flipside vias and deep implant isolation.

2.4 MULTI-VALUED LOGIC CIRCUIT DEVELOPMENT

In order to further demonstrate the feasibility of MVL with RTD's, two MVL circuits were designed, simulated and tested in hybrid form by the University of Michigan. They are a 4-step counter and a 4:1 multiple-valued multiplexer. Both circuits functioned as designed and provided substantial reductions in the number of circuit elements required compared to an equivalent circuit implemented with conventional digital logic elements.

The complete circuit diagram for the multiple-valued counter is shown in Figure 2-24. The design requires only three transistors and a single 4-peak RTD. An equivalent counter executed with 2-bit CMOS components would require more than 30 transistors. An NDR-SPICE simulation of the circuit was carried out to evaluate its performance at 0.5 GHz. The simulated input and output are shown in Figure 2-25. The behavior of the actual hybrid circuit closely matched the simulation, as seen in the experimental result in Figure 2-26.

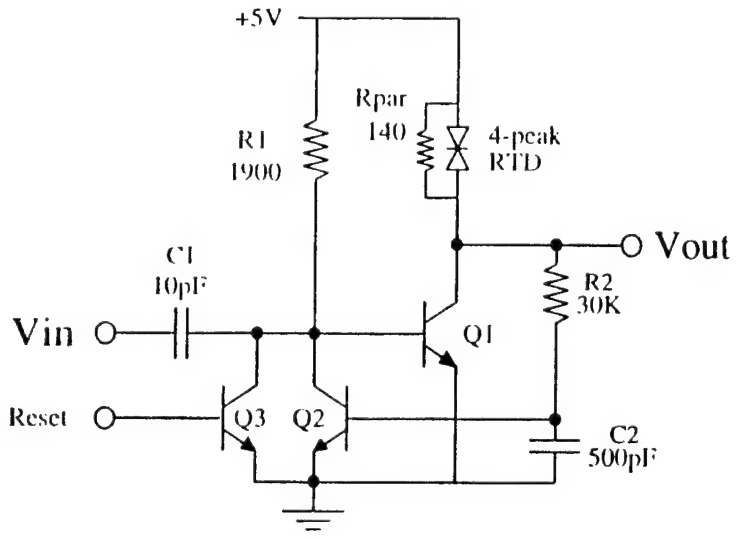


Figure 2-24. Circuit diagram of a multi-valued counter implemented with three transistors and a single RTD.

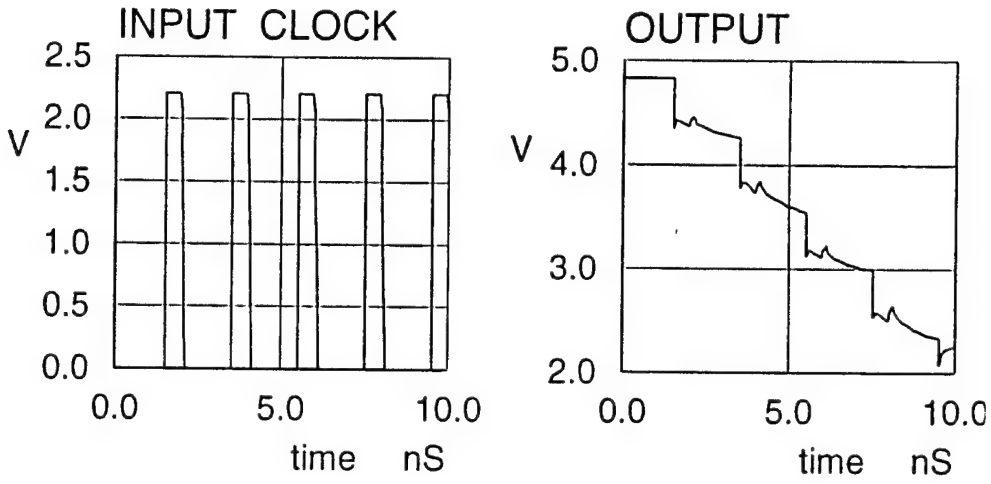


Figure 2-25. NDR-SPICE simulation at 0.5 GHz of the counter circuit in Figure 2-16.

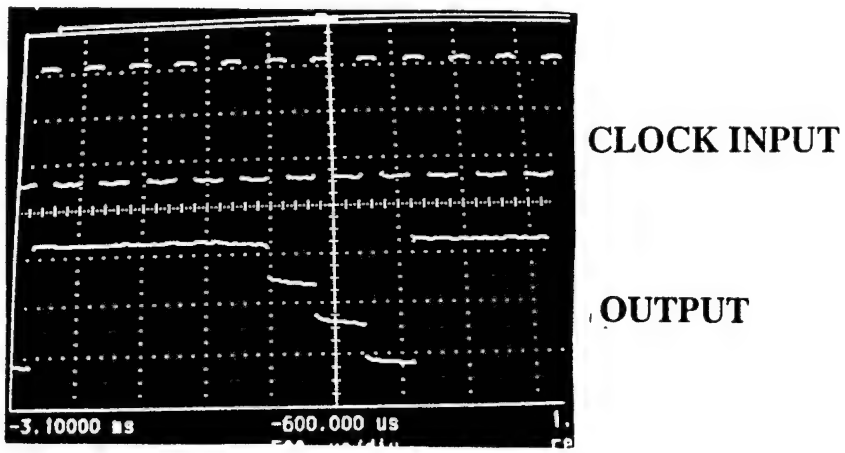


Figure 2-26. Experimental behavior of the multiple-valued counter hybrid circuit.

The 4:1 MVL multiplexer circuit is diagrammed in Figure 2-27. The design requires only twenty-one transistors and four RTD's. Circuit simulations indicate an ultimate power consumption of only 310 mW at a projected speed of 0.5 GHz. This RTD multiplexer design was breadboarded and tested as a decoder and an analog multiplexer. Figure 2-28 shows decoder operation of the circuit with the indicated "ENABLE" lines going low at their corresponding "SELECT" voltages. Note that the active low signals do not overlap, which is desirable for a decoder. The behavior of the circuit as an analog multiplexer is shown in Figure 2-29. As with the 4-step counter, the use of multiple-valued RTD's provides the desired functionality with significant reductions in circuit complexity.

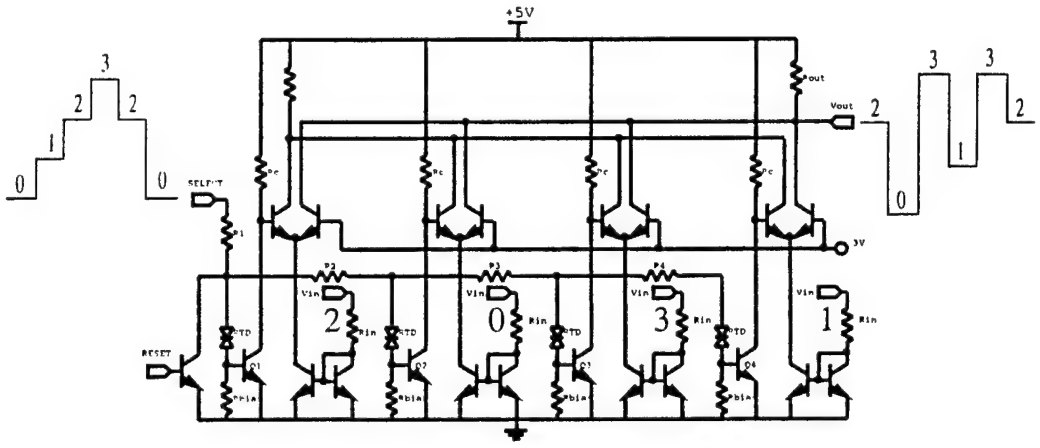


Figure 2-27. Circuit diagram of a 4:1 multiple-valued multiplexer requiring only 21 transistors and 4 RTD's.

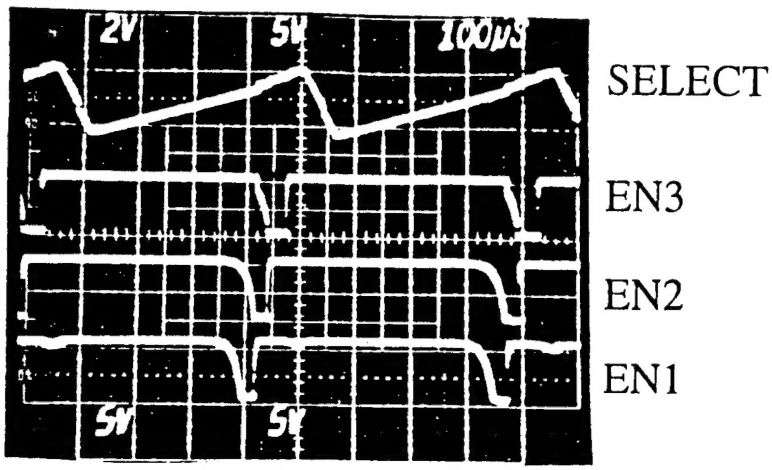
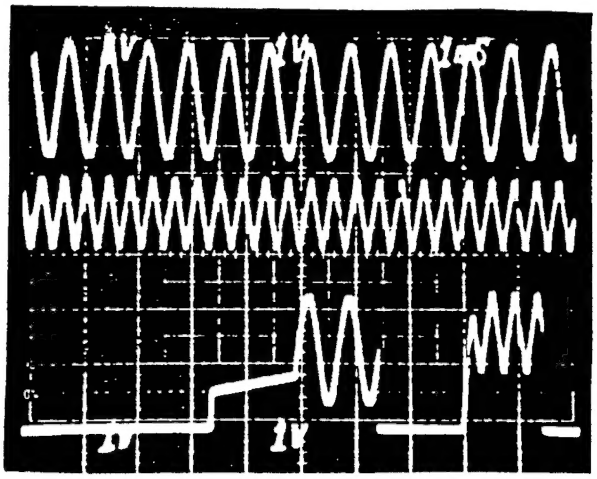


Figure 2-28. Experimental behavior of hybrid MVL multiplexer circuit operated as a decoder.



Channel 1 : Ramping up signal (Same as SELECT)
Channel 2 : Sinusoidal Wave
Channel 3 : Ground
Channel 4 : Triangular Wave

Figure 2-29. Experimental behavior of hybrid MVL multiplexer circuit operated as a 4:1 analog multiplexer.

2.5 CONCLUSION

The objective of the program was to develop multiple value logic for a 2:1 reduction in circuit complexity and a 2:1 increase in circuit speed. The approach was to achieve modulo-4 arithmetic in circuits based on resonant tunneling bipolar transistors (RTBT's). Because the multiple value functionality is integrated into the individual devices within the circuits, reductions in circuit complexity and propagation delays may be realized that might not otherwise be achieved. *DEN-MAT* and *QHD-CAD* algorithm were used to model devices and predict electrical behavior. MBE and GSMBE were used to grown epitaxial structures that included AlGaAs-GaAs and InGaP-GaAs heterojunction bipolar transistors (HBT's) integrated with multiple barrier AlAs-GaAs-InGaAs resonant tunnel diodes (RTD's). Collaborations were with Scientific Research Associates and the University of Michigan for device and circuit design, and with Georgia Tech for device characterization.

Three RTD designs were demonstrated with peak to valley rations of 6 at 300K. An RTBT (HBT integrated with an RTD) was fabricated that exhibited a bandwidth of 30 GHz. In addition, a novel epitaxial structure was proposed based upon a "collector-up" RTBT configuration that will greatly simplify the processing involved in the monolithic integration of RTD's and HBT's in multi-valued circuits. Finally, two multi-valued circuits were designed, simulated and tested in hybrid form. These were a 4-step counter and a 4:1 multiple valued multiplexer. Both functioned as designed. The counter, executed with only three transistors and one RTD, would have required more than thirty transistors to implement with binary CMOS logic circuitry.

Participating Scientific Personnel

Dr. J.M. Ballingall, Dr. T.J. Rogers, Mr. R.W. Yanka, Dr. L.W. Yang, Dr. H.L. Grubin, Prof. J. Laskar

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